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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 09/830,376
Filing Date: April 25, 2001
Appellant(s): SATOH, YOSHIKAZU

Michael Ure
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed July 16, 2007 appealing from the Office action mailed February 12, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is incorrect. A correct statement of the status of the claims is as follows:

This appeal involves claims 1, 3, 4, 6-7, 9-16, and 18.

Claims 2, 5, 8, and 17 are canceled.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The claim Appendix, on page 19, incorrectly labeled claim 9 as claim 10. In other words, two claims are labeled claim 10 on page 19. The first one should be labeled claim 9 while the second remains claim 10. Accordingly, claim 9 is correctly labeled in the Appendix to the Examiner's Answer.

On page 21 of the brief, claim 17 is shown dependent upon claim 17. However, claim 17 was previously canceled. This claim should be renumbered as claim 18 and should instead be dependent upon claim 16.

(8) Evidence Relied Upon

6,826,181	HIGASHIDA	03-1999
5,995,080	BIRO	06-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in a patent granted on an application for patent by another filed in the United States before the invention thereof by the applicant for patent, or on an international application

by another who has fulfilled the requirements of paragraphs (1), (2), and (4) of section 371(c) of this title before the invention thereof by the applicant for patent.

Claims 1, 3, and 15-16, and 18 are rejected under 35 U.S.C. 102(e) as being anticipated by Higashida et al. (6,826,181).

As per claim 1, Higashida et al. discloses a data writing/reading method of sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39]; wherein when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row

direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60; Fig. 23; col. 26, lines 55-63], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed; reading is executed in a unit in the column direction*; Fig.20, col.23, lines 38-46; Fig. 23; col. 26, lines 55-63].

As per claim 3, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 15, Higashida et al. discloses a memory for sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and*

sequentially reads the data; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

As per claim 16, Higashida et al. discloses a memory drive apparatus [*transmission and storage apparatus*; col.3, lines 45-48]; sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the

memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

As per claim 18, Higashida et al. discloses the apparatus provides with addressing means for addressing the memory [*the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67]; plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 4, 6-7, and 9-14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Higashida et al. (6,826,181) in view of Biro et al. (5,995,080).

As per claim 4, the rationale in the rejection of claim 1 above is herein incorporated. Higashida et al. further discloses a data writing/reading method of sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix*; col.3, lines 35-39].

However Higashida et al. does not explicitly teach a method of de-interleaving. Biro et al. discloses a method of de-interleaving [*a method for providing de-interleaving of data using a storage device*; col.2, lines 63-65] to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12).

Since the technology for implementing a storage system with a method of de-interleaving was well known as evidenced by Biro et al., and since a method of de-interleaving in a storage system provides output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware, an artisan would have been motivated to implement this feature in the system of Higashida et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made by applicant, to modify the system of Higashida et al. to include a method of de-interleaving because it was well known to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12) as taught by Biro et al..

As per claim 6, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of

each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 7, the rationale in the rejection of claim 1 above is herein incorporated. Higashida et al. further discloses a data processing method (Fig.4, *data processing circuit 104*; col.6, lines 42-43; *the transmission can be achieved by executing the process twice;* col.22, lines 33-34]; a first step of interleaving a plurality of data [*data into a plurality of blocks; a first processing means for executing a first interleave process*; col.3, lines 43-47]; sequentially writing a plurality of data into a memory in a write direction [*the generating means executes the interleave process by writing the data*; col.3, lines 34-35; *buffer memory 3000 in a first direction (write direction of Fig.21 (C)*; col.24, lines 50-51; *data into a plurality of blocks (plurality of data)*; col.2, lines 46-47]; and sequentially reading the plurality of data written into the memory in a read direction [*for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data*; col.21, lines 65-67; *memory 3000 in a second direction (read direction of Fig. 21(C))*; col.24, lines 53-55; *data into a plurality of blocks*; col.2, lines 46-47]; characterized in that a first plurality of data is written into the memory in a first write direction [*writing the data into the storage apparatus having a matrix form in a first direction*; col.3, lines 35-37]; the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *writing the*

data into a storage apparatus having a matrix form in a first direction, reading from the storage apparatus the data in a second direction perpendicular to the first direction of the matrix; col.3, lines 35-39].

However, Higashida et al. does not explicitly teach a second step of de-interleaving. Biro et al. discloses a second step of de-interleaving [to *provide de-interleaving, the first order of bytes includes a plurality of interleaved bytes of different types of data, and the second output order of bytes comprises a plurality of bytes of the same type of data;* col.3, lines 1-4] to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12).

Since the technology for implementing a storage system with a second step of de-interleaving was well known as evidenced by Biro et al., and since a second step of de-interleaving in a storage system provides output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware, an artisan would have been motivated to implement this feature in the system of Higashida et al.. Thus, it would have been obvious to one of ordinary skill in the art at the time invention was made by applicant, to modify the system of Higashida et al. to include a second step of de-interleaving because it was well known to provide output data that is stored in an interleaved format to other logic in a block format while using a minimal amount of additional hardware (col.3, lines 8-12) as taught by Biro et al..

As per claim 9, Higashida discloses the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix

form, and contains interleaving the plural data configuring the super frame [*execute the interleave process by writing data into a storage having a matrix form*; col.3, lines 34-37; *a first interleave processing means for executing a first interleave process by writing data into a first storage having a first matrix form; second interleave processing means for executing a second interleave process by writing data into a second storage having a second matrix form; each storage (frame) stores matrix/matrices which store(s) plural data*; col3, lines 46-61].

As per claim 10, Higashida et al. discloses plural data are arranged into the memory in matrix structures having n by n blocks [*a storage apparatus having a matrix form*; col.3, lines 36-37]; each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks [*when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases*; col.38, lines 6-9].

As per claim 11, Higashida et al. discloses when plural data having written into the memory at present are read in a row direction, plural data which is the next to be written are sequentially written in the row direction [*packet transmission (plurality of data)*; col.3, lines 27-28; *128-bytes data is written into memory 1002 in the row direction 9001 of Fig.17 and executes the writing of data*; col.21, lines 57-60], on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction [*data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the*

row direction of the next column is executed; reading is executed in a unit in the column direction;

Fig.20, col.23, lines 38-46].

Regarding claim 11, although Higashida et al. and Biro et al. do not explicitly teach each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data, such limitations are merely a matter of design choice and would have been obvious in the system of Higashida et al.. Higashida et al. teaches a two-dimensional matrix, and the frames become the multiple of 48 bytes to execute the interleave process and express data write and read control. The limitations in claim 11 do not define a patentably distinct invention over that in Higashida et al. since both the invention as a whole and Higashida et al. are directed to configuring and interleaving the super frame. The size of the data in the matrix is inconsequential for the invention as a whole and presents no new or unexpected results, as long as the data is in matrix form. Therefore, to have each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data would have been a matter of obvious design choice to one of ordinary skill in the art.

As per claims 12-14, the rationale in the rejection of claim 10 is herein incorporated.

Regarding claims 12-14, although Higashida et al. and Biro et al. do not explicitly teach a super frame having eight frames, each of the frames formed by arranging

(203x48) data in matrix form, interleaving (203x48x8) data, and each block having 4 or 26 addresses, such limitations are merely a matter of design choice and would have been obvious in the system of Higashida et al.. Higashida et al. teaches a two-dimensional matrix, and the frames become the multiple of 48 bytes, to execute the interleave process and express data write and read control, and control circuit 1003 generates an address to sequentially read the data in the row direction of the matrix. The limitations in claims 12-14 do not define a patentably distinct invention over that in Higashida et al. since both the invention as a whole and Higashida et al. are directed to configuring, interleaving the super frame, and sequentially reading the data. The size of the data in the matrix is inconsequential for the invention as a whole and presents no new or unexpected results, as long as the data is in matrix form. Therefore, to have each of the frames formed by arranging (203x48) data in matrix form, and interleaving (203x48x8) data would have been a matter of obvious design choice to one of ordinary skill in the art.

(10) Response to Argument

Appellant's arguments on page 15 that in Higashida there is no teaching or suggestion of "alternating the writing and reading directions so as to avoid the need for double-buffering". That is, there is no teaching or suggestion of "when plural data having been written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, and on the other hand, when plural data having been written into the memory at present are read in a column

direction, plural data which is the next to be written are sequentially written in the column direction", recited in independent claims 1, 15, and 16, is clearly erroneous.

Contrary to appellant's assumption, Figures 15 and 17 of Higashida clearly show an interleave buffer memory 1002 executing an interleave method in which "data are written in a unit of 124 bytes (0 to 123) in the row direction; col. 20, lines 55-56" and "the reading is executed in the column direction; col. 20, lines 63-64"; "128-bytes of data is written into memory 1002 in a row direction 9001 and execute the writing of the data; when the writing of each row is completed, the write operation is advanced in the row direction in a direction in which the column address increases, and the operation is switched to the reading; for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data so that data are read out in the column direction; [col. 21, ll 57-60]"; "where data are sequentially written in the row direction, and when the writing of data into each row is completed, writing of data in the row direction of the next column is executed [Fig. 20, col. 23, ll 38-46]"; "when the writing of data into each column is completed, the writing is advanced in the column direction of the data in a direction in which the row address increases [col. 38, ll 6-9]"; "for the reading, the interleave control circuit 1003 generates an address and sequentially reads the data [col. 21, ll 65-67]"; Figure 23 unequivocally shows "data string 1804 being written in the column direction into the interleave buffer memory 3000, and then is read out from the interleave buffer memory 3000 in the row direction; the read data is written in the row direction and then is read in the column direction; col. 26, lines 55-62."

Appellant argues as though the claims recite "alternating the writing and reading directions so as to avoid the need for double buffering". However, appellant is doing nothing but reading limitations of the specification into the claims to thereby narrow the scope of the claims by implicitly adding disclosed limitations which have no express basis in the claims. This is impermissible importation of subject matter from the specification into the claim and such is not in accordance with the MPEP. See MPEP 2111. See also *In re Morris*, 127 F.3d 1048, 1054-55, 44 USPQ2d 1023, 1027-28 (Fed. Cir. 1997).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Mardochee Chery
Examiner

Conferees:

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APPENDIX: THE CLAIMS ON APPEAL

1. A data writing/reading method of sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory, at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written ha the column direction.

3. A data writing/reading method as claimed in claim 1, wherein plural data are arranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

4. A method of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in

a read direction, characterized in that a first plurality of data is written into the memory into a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present ,are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

6. A de-interleaving method as claimed in claim 4, wherein plural data are arranged into the memory ha matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

7. A data processing method comprising a first step of interleaving a plurality of data, and a second step of de-interleaving by sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality Of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is

equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present axe read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

9. A data processing method as claimed in claim 7, wherein the first step contains configuring a super frame having plural frames, each of the frames formed by arranging plural data in matrix form, and contains interleaving the plural data configuring the super frame.

10. A data processing method as claimed in claim 7, wherein the second step is characterize in that interleaved plural data are arranged into the memory in matrix structures having u by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

11. A data processing method as claimed in claim 10, wherein the first step is characterized by configuring a super frame having eight frames, each of tile frames formed by arranging (203x48) data in matrix form, and is characterized by interleaving (203x48xS) data configuring the super frame, and the second step is characterized in that when (203x48x8) data having written into the memory at present are read in a row

direction, (203x48x8) data which is the next to be written are sequentially written in the row direction, on the other hand, when (203x48xS) data having written into the memory at present are read in a column direction, (203x48xS) data which is the next to be written are sequentially written in the column direction.

12. A data processing method as claimed in claim 11, wherein the second step is for arranging (203x48x8) data into the memory in 48 matrix structures, each of the 48 matrix structures formed from (203x8) data, and each of the 48 matrix structures is the structure having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.

13. A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 26 addresses, and each of the blocks for writing one data into an area corresponding to the one address of each of the blocks, mad the second step is for writing one data into the area corresponding to the one address of each of the blocks.

14. A data processing method as claimed in claim 12, wherein each of the 48 matrix structures is the structure having 8 by 8 blocks, each of the blocks having 4 addresses, and each of the blocks for writing 7 data into an area corresponding to the one address

of each of the blocks, and the second step is for writing 7 data into the area corresponding to the one address of each of the blocks.

15. A memory for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

16. A memory drive apparatus for sequentially writing a plurality of data into a memory in a write direction, and sequentially reading the plurality of data written into the memory in a read direction, characterized in that a first plurality of data is written into the memory in a first write direction, the first plurality of data being read from the memory in a first read direction different from the first write direction, a second plurality of data being written after the first plurality of data in a second write direction which is equal to or is opposite to the first read direction; wherein when plural data having written into the

memory at present are read in a row direction, plural data which is next to be written are sequentially written in the row direction, on the other hand, when plural data having written into the memory at present are read in a column direction, plural data which is the next to be written are sequentially written in the column direction.

18. A memory drive apparatus as claimed in claim 16, wherein the apparatus provides with addressing means for addressing the memory, and by sequentially addressing the memory with the addressing means, plural data are rearranged into the memory in matrix structures having n by n blocks, each of the blocks having at least one address, and each of the blocks for writing at least one data into an area corresponding to the one address of each of the blocks.